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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,901	09/26/2003	Kazi Asaduzzaman	174/280	9181

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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,901	ASADUZZAMAN ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2/5/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2/5/2004 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

2. The abstract of the disclosure is objected to because applicant failed to list "ABSTRACT" or "ABSTRACT OF DISCLOSURE" as heading for their abstract. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-13, 15, and 18-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Kenney et al.(US Patent 6,803,827).

As to claim 1, Kenney et al. discloses circuitry(CDR 100, see Fig. 2) for providing a dynamically adjustable bandwidth(bandwidth, see column 6, line 42) comprising a phase frequency detector(phase detector 108a, see Fig. 3) receiving as input a clock

signal(1st reference signal 120a, see Fig. 3) and having a signal output, a charge pump(charge pump 114, see Fig. 3) having a pump input coupled to the signal output of the phase frequency detector and having a pump output, and a loop filter(loop filter 110, see Fig. 3) input coupled to the pump output of the charge pump and having a filter output. Kenney also discloses a voltage controlled oscillator(tunable oscillator 112a, see Fig. 3) having an oscillator input coupled to the filter output of the loop filter and having an oscillator output(signal 122, see Fig. 2), a divider circuit(frequency divider circuit 162, see Fig. 3) having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector, and control circuitry(frequency detector circuit 190, see Fig. 4) that receives as input at least one control signal(FDLOCKB 197, see Fig. 4) and is operative to dynamically adjust a setting in at least one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit while the circuitry is processing data.

As to claim 2, Kenney discloses the circuitry wherein the circuitry is clock data recovery circuitry(CDR 100a, see Fig. 3).

As to claim 3, Kenney discloses the circuitry wherein the circuitry is phase locked loop circuitry(phased-locked loop 102a, see Fig. 3).

As to claim 4, Kenney discloses the circuitry wherein the setting in the charge pump that can be dynamically adjusted is current(current sources 150 and 152, see Fig. 3; and column 6, lines 65-66).

As to claim 5, Kenney discloses the circuitry wherein the setting in the loop filter that can be dynamically adjusted is at least one of a resistor value(resistor 116, see Fig. 3) and a capacitor value(capacitor 118, see Fig. 3).

As to claim 6, Kenney discloses the circuitry wherein the setting in the voltage controlled oscillator that can be dynamically adjusted is a voltage gain(*Vcourse,* 115a, see Fig. 3).

As to claim 7, Kenney discloses the circuitry wherein the setting in the divider circuit that can be dynamically adjusted is a scale factor(see column 7, lines 5-9).

As to claim 8, Kenney discloses the circuitry wherein the at least one control signal includes a value for the setting(see column 8, lines 46-48).

As to claim 9, Kenney discloses the circuitry wherein the at least one control signal is indicative of whether a value of the setting is to be increased or decreased(see column 7, lines 62-67).

As to claim 10, Kenney discloses the circuitry wherein the at least one control signal includes at least one data bit that corresponds to information on a value for the setting stored in a lookup table in the control circuitry(see column 8, lines 10-24).

As to claim 11, Kenney discloses the circuitry wherein the at least one control signal set by a programmable logic device(programmable register 216, see Fig. 5A).

As to claim 12, Kenney discloses the circuitry wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 8, lines 24-32).

As to claim 13, Kenney discloses the circuitry wherein the at least one control signal is set by user input(reference clock 120a, see Fig. 3).

As to claim 15, Kenney discloses a printed circuit board on which is mounted the previously defined apparatus(see column 1, lines 64-66).

As to claim 18, Kenney discloses a programmable logic device comprising clock data recovery (CDR) circuitry(CDR 100, see Fig. 2) that receives as input a reference clock signal(1st reference signal 120a, see Fig. 3) and a CDR signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal, and to use the recovered clock signal to recover clock information and data information from the CDR signal(see column 5, lines 10-16). Kenney also discloses the programmable logic device comprising control circuitry(frequency detector circuit 190, see Fig. 4) that receives as input at least one control signal(FDLOCKB 197, see Fig. 4) and is operative to dynamically adjust a bandwidth(bandwidth, see column 6, line 42) of the CDR circuitry by changing a setting in at least one component in the CDR circuitry while the CDR circuitry is processing data.

As to claim 19, Kenney discloses the programmable logic device wherein the CDR circuitry comprises a phase frequency detector(phase detector 108a, see Fig. 3) receiving as input the reference clock signal having a signal output, a charge pump(charge pump 114, see Fig. 3) having a pump input coupled to the signal output of the phase frequency detector and having a pump output, and a loop filter(loop filter 110, see Fig. 3) having a filter input coupled to the pump output of the charge pump and

having a filter output. Kenney also discloses a voltage controlled oscillator(tunable oscillator 112a, see Fig. 3) having an oscillator input coupled to the filter output of the loop filter and having an oscillator output(signal 122, see Fig. 2), and a divider circuit(frequency divider circuit 162, see Fig. 3) having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

As to claim 20, Kenney discloses the programmable logic device wherein the at least one component comprises one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit(see column 5, lines 44-49).

As to claim 21, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises current(current sources 150 and 152, see Fig. 3; and column 6, lines 65-66) in the charge pump.

As to claim 22, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a resistor value(resistor 116, see Fig. 3) in the loop filter.

As to claim 23, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a capacitor value(capacitor 118, see Fig. 3) in the loop filter.

As to claim 24, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a voltage gain(*Vcourse,* 115a, see Fig. 3) in the voltage controlled oscillator.

As to claim 25, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a scale factor in the divider circuit(see column 7, lines 5-9).

As to claim 26, Kenney discloses the programmable logic device wherein the at least one control signal is set by the programmable logic device(programmable register 216, see Fig. 5A).

As to claim 27, Kenney discloses the programmable logic device wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 8, lines 24-32).

As to claim 28, Kenney discloses the programmable logic device wherein the at least one control signal is set by the user input(reference clock 120a, see Fig. 3).

As to claim 29, Kenney discloses a programmable logic device comprising phase lock loop (PLL) circuitry(phased-locked loop 102a, see Fig. 3) that receives as input a reference clock signal(1st reference signal 120a, see Fig. 3) and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal. Kenney further discloses the programmable logic device comprising control circuitry(frequency detector circuit 190, see Fig. 4) that receives as input at least one control signal(FDLOCKB 197, see Fig. 4) and is operative to dynamically adjust a bandwidth(bandwidth, see column 6, line 42) of the PLL circuitry by changing a setting in at least one component in the PLL circuitry while the PLL circuitry is processing data.

As to claim 30, Kenney discloses the programmable logic device wherein the PLL circuitry comprises a phase frequency detector(phase detector 108a, see Fig. 3) receiving as input the reference clock signal having a signal output, a charge pump(charge pump 114, see Fig. 3) having a pump input coupled to the signal output of the phase frequency detector and having a pump output, and a loop filter(loop filter 110, see Fig. 3) having a filter input coupled to the pump output of the charge pump and having a filter output. Kenney also discloses a voltage controlled oscillator(tunable oscillator 112a, see Fig. 3) having an oscillator input coupled to the filter output of the loop filter and having an oscillator output(signal 122, see Fig. 2), and a divider circuit(frequency divider circuit 162, see Fig. 3) having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

As to claim 31, Kenney discloses the programmable logic device wherein the at least one component comprises one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit(see column 5, lines 44-49).

As to claim 32, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises current(current sources 150 and 152, see Fig. 3; and column 6, lines 65-66) in the charge pump.

As to claim 33, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a resistor value(resistor 116, see Fig. 3) in the loop filter.

As to claim 34, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a capacitor value(capacitor 118, see Fig. 3) in the loop filter.

As to claim 35, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a voltage gain(*Vcourse,* 115a, see Fig. 3) in the voltage controlled oscillator.

As to claim 36, Kenney discloses the programmable logic device wherein the setting in the at least one component comprises a scale factor in the divider circuit(see column 7, lines 5-9).

As to claim 37, Kenney discloses the programmable logic device wherein the at least one control signal is set by the programmable logic device(programmable register 216, see Fig. 5A).

As to claim 38, Kenney discloses the programmable logic device wherein the at least one control signal is set by circuitry external to the programmable logic device(see column 8, lines 24-32).

As to claim 39, Kenney discloses the programmable logic device wherein the at least one control signal is set by the user input(reference clock 120a, see Fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 14, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kenney et al.(US Patent 6,803,827) further in view of Brunn et al.(US Patent 6,650,195).

As to claim 14, Kenney discloses a digital processing system comprising previously defined circuitry. However Kenney fails to disclose the previously defined circuitry coupled to processing circuitry and memory coupled to the processing circuitry.

Brunn et al teaches a digital processing system(Exemplary system 500, see Fig. 5) comprising processing circuitry(CPUs 512 and 522, see Fig. 5)) and memory(Memories 514 and 524, see Fig. 5) coupled to the processing circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Kenney and Brunn in order to complete the digital processing system comprising processing circuitry and memory with circuitry consisting of a phase frequency detector, charge pump, loop filter, VCO, divider circuit, and control circuitry. Motivation to do so would be to be able to dynamically adjust bandwidth within the digital processing system.

As to claim 16, Kenney discloses the printed circuit board. However Kenney fails to disclose the printed circuit board further comprising a memory mounted on the printed circuit board and coupled to the circuitry.

Brunn teaches a memory(memories 514 and 524, see Fig. 5) mounted on the printed circuit board and coupled to the circuitry.

As to claim 17, Kenney discloses the printed circuit board. However, Kenney fails to disclose the printed circuit board comprising processing circuitry mounted on the printed circuit board and coupled to the apparatus.

Brunn teaches the processing circuitry(CPUs 512 and 524, see Fig. 5) mounted on the printed circuit board and coupled to the apparatus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

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